IN THE CLAIMS:

19. (originally presented) In a computer controlled system having a processor operating according to a clock and an updatable table operating asynchronously of the clock, the updatable table outputting control data for controlling data transfers in the system, an apparatus, comprising:

a memory receiving update data from the processor during a first time period at a data rate corresponding to the clock and outputting the update data to the updatable table;

a control circuit coupled to the memory, wherein the control circuit determines the beginning of a second period of time during which the updatable table is not being used and updates the updatable table during the second period, asynchronously with the clock, using at least some of the update data.

20. (originally presented) Apparatus, as claimed in line 19, further comprising a plurality of shadow registers wherein data stored in the memory at a first storage time is also stored in at least one of the plurality of shadow registers substantially simultaneously with the first storage time.

21. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table comprises an updatable transmit table and updatable receive table, and wherein the memory includes at least a transmit holding memory for holding data for updating the updatable transmit table and a receive holding memory, different from the transmit holding memory, for holding data for updating the updatable receive table.

22. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table comprises a switch table.

23. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table comprises a routing table.

24. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table controls the routing of isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, on a bus.

25. (originally presented) Apparatus, as claimed in claim 24, wherein the isochronous data comprises telephony data, video data, or a combination of telephony data and video data.

26. (originally presented) Apparatus, as claimed in claim 24, wherein the non-isochronous data comprises packet data.

27. (originally presented) Apparatus, as claimed in claim 24, wherein the non-isochronous data comprises Ethernet data.

28. (originally presented) Apparatus, as claimed in claim 24, wherein the non-isochronous data comprises non-packet, non-isochronous data.

29. (originally presented) Apparatus, as claimed in claim 24, wherein the non-isochronous data comprises ATM data.

30. (originally presented) Apparatus, as claimed in claim 24, wherein the bus comprises a time division multiplexed bus.

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31. (originally presented) Apparatus, as claimed in claim 24, wherein the bus comprises a time slot interchange bus.

32. (originally presented) Apparatus, as claimed in claim 24, wherein the bus comprises a bus for carrying ATM, SONET or 1394 data.

33. (originally presented) Apparatus, as claimed in claim 24, wherein the bus connects multiple hubs in the system.

34. (originally presented) Apparatus, as claimed in claim 19, wherein the memory comprises a register.

35. (previously amended) Apparatus, as claimed in claim 19, wherein the memory comprises a random access memory (RAM).

36. (originally presented) Apparatus, as claimed in claim 19, wherein the memory comprises a multi-port memory.

37. (originally presented) Apparatus, as claimed in claim 19, wherein update data is transferred to the memory in the form of a burst.

38. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table operates synchronously with a second clock.

39. (originally presented) Apparatus, as claimed in claim 38, wherein the second clock comprises a network reference clock.

40. (originally presented) Apparatus, as claimed in claim 39, wherein the network reference clock comprises a WAN reference clock.

41. (originally presented) Apparatus, as claimed in claim 39, wherein the network reference clock comprises a LAN reference clock.

42. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table controls a hub in the system.

43. (originally presented) Apparatus, as claimed in claim 42, wherein the hub comprises a PBX.

44. (originally presented) Apparatus, as claimed in claim 42, wherein the hub includes multiple LAN connections.

45. (originally presented) Apparatus, as claimed in claim 42, wherein the hub includes multiple isochronous switching devices.

46. (originally presented) Apparatus, as claimed in claim 42, wherein the hub includes multiple Ethernet connections.

47. (originally presented) Apparatus, as claimed in claim 42, wherein the hub is coupled to multiple nodes.

48. (originally presented) Apparatus, as claimed in claim 47, wherein each of the nodes transfers isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, in the system under control of the updatable table.

49. (originally presented) Apparatus, as claimed in claim 19, wherein data transfer in the system is controlled so that bandwidth for isochronous data transfers is insensitive to a level of non-isochronous data transfers in the system.

50. (originally presented) Apparatus, as claimed in claim 19, wherein data transfer in the system is controlled so that bandwidth for non-isochronous data transfers is insensitive to a level of isochronous data transfers in the system.

51. (originally presented) Apparatus, as claimed in claim 19, wherein operations that the processor handles includes call control, signaling, maintenance activities, status processing, and error bookkeeping.

52. (originally presented) Apparatus, as claimed in claim 19, wherein the update data comprises data transmitted over a D channel.

53. (currently amended) In a computer-controlled system having a processor operating according to a clock and an updatable table operating asynchronously with the clock, the

updatable table outputting control data for controlling data transfers in the system, a method, comprising:

receiving update data in a memory from the processor during a first time period at a data rate corresponding to the clock and outputting the update data to the updatable table; and

determining the beginning of a second period of time during which the updatable table is not being used and updating the updatable table during the second period of time, asynchronously with the clock, using at least some of the update data.

54. (originally presented) A method, as claimed in claim 53, wherein the update data includes at least one control word, indicating a table update location, and at least one data word, including data to be stored at the update location.

55. (originally presented) A method, as claimed in claim 54, wherein the update data includes more data words than control words.

56. (originally presented) A method, as claimed in claim 55, further comprising the step of incrementing the control word by a first amount to provide a new table update location for a subsequent table update.

57. (previously amended) A method, as claimed in claim 56, wherein the first amount is programmable.

58. (originally presented) A method, as claimed in claim 53, wherein the update data includes a plurality of words, each of the plurality of words having at least one bit indicating whether the word is a control word or a data word.

59. (originally presented) A method, as claimed in claim 53, wherein the update data includes a plurality of words, each of the plurality of words having at least one bit indicating whether the word is the last data word of the update data.

60. (originally presented) A method, as claimed in claim 53, further comprising the step of notifying the processor when the table update is complete.

61. (originally presented) A method, as claimed in claim 60, wherein the step of notifying comprises sending an interrupt to the processor.

62. (originally presented) A method, as claimed in claim 60, wherein, after the processor has written the update data into the memory, the processor is prevented from writing further data into the memory until after the step of notifying.

63. (originally presented) A method, as claimed in claim 53, wherein the updatable table comprises a switch table.

64. (originally presented) A method, as claimed in claim 53, wherein the updatable table comprises a routing table.

65. (originally presented) A method, as claimed in claim 53, wherein the updatable table controls the routing of isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, on a bus.

66. (originally presented) A method, as claimed in claim 65, wherein the isochronous data comprises telephony data, video data, or a combination of telephony data and video data.

B2 67. (originally presented) A method, as claimed in claim 65, wherein the non-isochronous data comprises packet data.

68. (originally presented) A method, as claimed in claim 65, wherein the non-isochronous data comprises Ethernet data.

69. (originally presented) A method, as claimed in claim 65, wherein the non-isochronous data comprises non-packet, non-isochronous data.

70. (originally presented) A method, as claimed in claim 65, wherein the non-isochronous data comprises ATM data.

71. (originally presented) A method, as claimed in claim 65, wherein the bus comprises a time division multiplexed bus.

72. (originally presented) A method, as claimed in claim 65, wherein the bus comprises a time slot interchange bus.

73. (originally presented) A method, as claimed in claim 65, wherein the bus comprises a bus for carrying ATM, SONET or 1394 data.

74. (originally presented) A method, as claimed in claim 65, wherein the bus connects multiple hubs in the system.

75. (originally presented) A method, as claimed in claim 53, wherein the memory comprises a register.

76. (previously amended) A method, as claimed in claim 53, wherein the memory comprises a random access memory (RAM).

77. (originally presented) A method, as claimed in claim 53, wherein the memory comprises a multi-port memory.

78. (originally presented) A method, as claimed in claim 53, wherein update data is transferred to the memory in the form of a burst.

79. (originally presented) A method, as claimed in claim 53, wherein the updatable table operates synchronously with a second clock.

80. (originally presented) A method, as claimed in claim 79, wherein the second clock comprises a network reference clock.

81. (originally presented) A method, as claimed in claim 80, wherein the network reference clock comprises a WAN reference clock.

82. (originally presented) A method, as claimed in claim 80, wherein the network reference clock comprises a LAN reference clock.

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83. (originally presented) A method, as claimed in claim 53, wherein the updatable table controls a hub in the system.

84. (originally presented) A method, as claimed in claim 83, wherein the hub comprises a PBX.

85. (originally presented) A method, as claimed in claim 83, wherein the hub includes multiple LAN connections.

86. (originally presented) A method, as claimed in claim 83, wherein the hub includes multiple isochronous switching devices.

87. (originally presented) A method, as claimed in claim 83, wherein the hub includes multiple Ethernet connections.

88. (originally presented) A method, as claimed in claim 83, wherein the hub is coupled to multiple nodes.

89. (originally presented) A method, as claimed in claim 88, wherein each of the nodes transfers isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, in the system under control of the updatable table.

90. (originally presented) A method, as claimed in claim 53, wherein data transfer in the system is controlled so that bandwidth for isochronous data transfers is insensitive to a level of non-isochronous data transfers in the system.

91. (originally presented) A method, as claimed in claim 53, wherein data transfer in the system is controlled so that bandwidth for non-isochronous data transfers is insensitive to a level of isochronous data transfers in the system.

92. (originally presented) A method, as claimed in claim 53, wherein operations that the processor handles includes call control, signaling, maintenance activities, status processing, and error bookkeeping.

93. (originally presented) A method, as claimed in claim 53, wherein the update data comprises data transmitted over a D channel.

94. (currently amended) Apparatus for communicating between at least first and second stations in a data communication system over at least a first link, the data communication system including a plurality of data sources and sinks, at least a first of the sources and sinks configured to receive or transmit data isochronously and a second of the sources and sinks configured to transmit data non-isochronously, the apparatus comprising:

at least a receiver and at least a first transmitter in the first station;

the first link coupling the first station with the second station;

the second station being coupled to both the first and second of the sources and sinks;

a second transmitter in the second station for transmitting data to the first receiver;

a first multiplexer in the second station for permitting the transmitting of data from both of the first and second sources and sinks over the first link as first multiplexed data, the multiplexer providing a first bandwidth for first data originating from an isochronous source, including at least the first of the sources and sinks;

at least a first updatable switch table in the first station for storing information indicating at least the destination of data;

a processor operating according to a first clock, coupled to the updatable switch table, the updatable switch table operating according to a second clock asynchronously with the first clock;

a memory coupled to the processor receiving update data from the processor during a first time period at a data rate corresponding to the clock and coupled to the first updatable switch table and outputting the update data to the first updatable switch table.

95. (originally presented) Apparatus, as claimed in claim 94, wherein data transfer in the system is controlled so that bandwidth for isochronous data transfers is insensitive to a level of non-isochronous data transfers in the system.

96. (originally presented) Apparatus, as claimed in claim 94, wherein data transfer in the system is controlled so that bandwidth for non-isochronous data transfers is insensitive to a level of isochronous data transfers in the system.

97. (currently amended) A method for communicating data over a data link in a data communication system between a first station coupled to a first endpoint of the data link and a second station coupled to a second endpoint of the data link, the second station having an isochronous data source, a non-isochronous data source or both an isochronous data source and a non-isochronous data source, the data communication system having a time-varying amount of non-isochronous demand, the method comprising;

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time-division multiplexing data from the isochronous data source and/or the non-isochronous data source, wherein a first bandwidth is allocated for data from the isochronous source, wherein the data transfer rate for the isochronous data is substantially independent of the non-isochronous demand on the data system;

providing a processor in the first station operating according to a first clock and an updatable table operating according to a second clock asynchronously with the first clock;

receiving update data in a memory from the processor during a first time period at a data rate corresponding to the clock, the update data including at least destination data;

updating the updatable table asynchronously with the first clock, using at least some of the update data in the memory; and

transmitting the time-multiplexed data onto the data link in accordance with data stored in the updatable table.

98. (originally presented) A method, as claimed in claim 97, wherein the step of updating comprises:

sampling the second clock;

providing the sampled second clock to a circuit whose output has a corresponding relationship to the rising edge of the second clock.

99. (originally presented) A method, as claimed in claim 97, further comprising the step of:

waiting up to a predetermined maximum wait time before performing the step of receiving update data if fewer than a predetermined number of update words are contained in the update data.

100. (originally presented) A method, as claimed in claim 99, wherein the predetermined number of update words is equal to the number of words that can be stored in the memory.

101. (originally presented) A method, as claimed in claim 97, wherein the update data includes at least one control word, indicating a table update location, and at least one data word, including data to be stored at the update location.

102. (originally presented) A method, as claimed in claim 101, wherein the update data includes more data words than control words.

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103. (originally presented) A method, as claimed in claim 102, further comprising the step of incrementing the control word by a first amount to provide a new table update location for a subsequent table update.

104. (previously amended) A method, as claimed in claim 103, wherein the first amount is programmable.

105. (originally presented) A method, as claimed in claim 97, wherein the update data includes a plurality of words, each of the plurality of words having at least one bit indicating whether the word is a control word or a data word.

106. (originally presented) A method, as claimed in claim 97, wherein the update data includes a plurality of words, each of the plurality of words having at least one bit indicating whether the word is the last data word of the update data.

107. (originally presented) A method, as claimed in claim 97, further comprising the step of notifying the processor when the table update is complete.

108. (originally presented) A method, as claimed in claim 107, wherein the step of notifying comprises sending an interrupt to the processor.

109. (originally presented) A method, as claimed in claim 107, wherein, after the processor has written the update data into the memory, the processor is prevented from writing further data into the memory until after the step of notifying.

110. (originally presented) A method, as claimed in claim 97, wherein the updatable table comprises a switch table.

111. (originally presented) A method, as claimed in claim 97, wherein the updatable table comprises a routing table.

112. (originally presented) A method, as claimed in claim 97, wherein the updatable table controls the routing of isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, on a bus.

113. (originally presented) A method, as claimed in claim 112, wherein the isochronous data comprises telephony data, video data, or a combination of telephony data and video data.

114. (originally presented) A method, as claimed in claim 112, wherein the non-isochronous data comprises packet data.

115. (originally presented) A method, as claimed in claim 112, wherein the non-isochronous data comprises Ethernet data.

116. (originally presented) A method, as claimed in claim 112, wherein the non-isochronous data comprises non-packet, non-isochronous data.

117. (originally presented) A method, as claimed in claim 112, wherein the non-isochronous data comprises ATM data.

118. (originally presented) A method, as claimed in claim 112, wherein the bus comprises a time division multiplexed bus.

119. (originally presented) A method, as claimed in claim 112, wherein the bus comprises a time slot interchange bus.

120. (originally presented) A method, as claimed in claim 112, wherein the bus comprises a bus for carrying ATM, SONET or 1394 data.

121. (originally presented) A method, as claimed in claim 112, wherein the bus connects multiple hubs in the system.

122. (originally presented) A method, as claimed in claim 97, wherein the memory comprises a register.

123. (previously amended) A method, as claimed in claim 97, wherein the memory comprises a random access memory (RAM).

124. (originally presented) A method, as claimed in claim 97, wherein the memory comprises a multi-port memory.

125. (originally presented) A method, as claimed in claim 97, wherein update data is transferred to the memory in the form of a burst.

126. (originally presented) A method, as claimed in claim 97, wherein the updatable table operates synchronously with the second clock, the second clock having a different frequency than the first clock.

127. (originally presented) A method, as claimed in claim 97, wherein the second clock comprises a network reference clock.

128. (originally presented) A method, as claimed in claim 127, wherein the network reference clock comprises a WAN reference clock.

B2 129. (originally presented) A method, as claimed in claim 127, wherein the network reference clock comprises a LAN reference clock.

130. (originally presented) A method, as claimed in claim 97, wherein the updatable table controls a hub in the system.

131. (originally presented) A method, as claimed in claim 130, wherein the hub comprises a PBX.

132. (originally presented) A method, as claimed in claim 130, wherein the hub includes multiple LAN connections.

133. (originally presented) A method, as claimed in claim 130, wherein the hub includes multiple isochronous switching devices.

134. (originally presented) A method, as claimed in claim 130, wherein the hub includes multiple Ethernet connections.

135. (originally presented) A method, as claimed in claim 130, wherein the hub is coupled to multiple nodes.

136. (originally presented) A method, as claimed in claim 135, wherein each of the nodes transfers isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, in the system under control of the updatable table.

137. (originally presented) A method, as claimed in claim 97, wherein data transfer in the system is controlled so that bandwidth for isochronous data transfers is insensitive to a level of non-isochronous data transfers in the system.

138. (originally presented) A method, as claimed in claim 97, wherein data transfer in the system is controlled so that bandwidth for non-isochronous data transfers is insensitive to a level of isochronous data transfers in the system.

139. (originally presented) A method, as claimed in claim 97, wherein operations that the processor handles includes call control, signaling, maintenance activities, status processing, and error bookkeeping.

140. (originally presented) A method, as claimed in claim 97, wherein the update data comprises data transmitted over a D channel.

PRESENTATION OF THE CLAIMS TO SHOW STATUS OF ALL CLAIMS AFTER THIS AMENDMENT AND TO SHOW CHANGES MADE TO CLAIMS NEWLY-ADDED IN THIS REISSUE

1. (original) In a computer-controlled system having a microprocessor operating according to a clock and an updatable table operating asynchronously of said clock, said updatable table outputting control data for controlling data transfer in said system, apparatus for updating said updatable table, comprising:

register means for receiving update data from said microprocessor during a first time period at a data rate corresponding to said clock and outputting said update data to said updatable table;

means, coupled to said register means, for determining the beginning of a second period of time during which said updatable table is not being used and for updating said updatable table during said second period, asynchronously with said clock, using at least some of said update data.

2. (original) Apparatus, as claimed in claim 1, further comprising a plurality of shadow registers wherein data stored in said register means at a first storage time is also stored in at least one of said plurality of shadow registers substantially simultaneously with said first storage time.

3. (original) Apparatus, as claimed in claim 1, wherein said updatable table comprises an updatable transmit table and updatable receive table, and wherein said register means includes at least a transmit holding register for holding data for updating said updatable transmit table and a receive holding register, different from said transmit holding register, for holding data for updating said updatable receive table.

4. (original) In a computer-controlled system having a microprocessor operating according to a clock and an updatable table operating asynchronously with said clock, said updatable table outputting control data for controlling data transfer in said system, a method for updating said updatable table, comprising:

receiving update data in a first register from said microprocessor during a first time period at a data rate corresponding to said clock and outputting said update data to said updatable table;

determining the beginning of a second period of time during which said updatable table is not being used and updating said updatable table during said second period of time during which

said updatable table is not being used, asynchronously with said clock, using at least some of said update data.

5. (original) A method, as claimed in claim 4, wherein said update data includes at least one control word, indicating a table update location, and at least one data word, including data to be stored at said update location.

6. (original) A method, as claimed in claim 5, wherein said update data includes more data words than control words.

7. (original) A method, as claimed in claim 6, further comprising incrementing said control word by a first amount to provide a new table update location for a subsequent table update.

8. (original) A method, as claimed in claim 7, wherein said first amount is programmable.

9. (original) A method, as claimed in claim 4 wherein said update data includes a plurality of words each of said plurality of words having at least one bit indicating whether the word is a control word or a data word.

10. (original) A method, as claimed in claim 4, wherein said update data includes a plurality of words each of said plurality of words having at least one bit indicating whether the word is the last data word of the update data.

11. (original) A method, as claimed in claim 4, further comprising notifying said microprocessor when the table update is complete.

12. (original) A method, as claimed in claim 11, wherein said step of notifying comprises sending an interrupt to said processor.

13. (original) A method, as claimed in claim 11, wherein, after said microprocessor has written said update data into said first register, said microprocessor is prevented from writing further data into said first register until after said step of notifying.

14. (original) Apparatus for communicating between at least first and second stations in a data communication system over at least a first link, said data communication system including a plurality of data sources and sinks, at least a first of said sources and sinks configured to receive or transmit data isochronously and a second of said sources and sinks configured to transmit data non-isochronously, the apparatus comprising:

at least a first receiver and at least a first transmitter in said first station;

said first link coupling said first station with said second station;

said second station being coupled to both said first and second of said sources and sinks;

a second transmitter in said second station for transmitting data to said first receiver;

a first multiplexer in said second station for permitting the transmitting of data from both of said first and second sources and sinks over said first link as first multiplexed data, said multiplexer providing a first, dedicated bandwidth for first data originating from an isochronous source, including at least said first of said sources and sinks;

at least a first updatable switchtable in said first station for storing information indicating at least the destination of data;

a microprocessor operating according to a first clock, coupled to said updatable switchtable, said updatable switchtable operating according to a second clock asynchronously with said first clock;

a register coupled to said microprocessor for receiving update data from said microprocessor during a first time period at a data rate corresponding to said first clock and coupled to said first updatable switchtable for outputting said update data to said first updatable switchtable.

15. (original) A method for communicating data over a data link in a data communication system between a first station coupled to a first endpoint of said data link and a second station coupled to a second endpoint of said data link, said second station having both an isochronous data source and a non-isochronous data source, said data communication system having a time-varying amount of non-isochronous demand, the method comprising;

time-division multiplexing data from said isochronous data source and said non-isochronous data source according to a periodically repeating frame structure, said frame structure defining at least a first dedicated bandwidth for data from said isochronous source, wherein the data transfer rate for said isochronous data is substantially independent of the non-isochronous demand on said data system;

providing a microprocessor in said first station operating according to a first clock and an updatable table operating according to a second clock asynchronously with said first clock;

receiving update data in a holding register from said microprocessor during a first time period at a data rate corresponding to said first clock, said update data including at least destination data;

updating said updatable table asynchronously with said first clock, using at least some of said update data in said holding register; and

transmitting the time-multiplexed data onto said data link in accordance with data stored in said updatable table.

16. (original) A method, as claimed in claim 15, wherein said step of updating comprises:

sampling said second clock;

providing said sampled second clock to a one-shot circuit whose output indicates the rising edge of said second clock.

17. (original) A method, as claimed in claim 15, further comprising:

waiting up to a predetermined maximum wait time before performing said step of receiving update data if fewer than a predetermined number of update words are contained in said update data.

18. (original) A method, as claimed in claim 17, wherein said predetermined number of update words is equal to the number of word that can be stored in said holding register.

19. (originally presented) In a computer controlled system having a processor operating according to a clock and an updatable table operating asynchronously of the clock, the updatable table outputting control data for controlling data transfers in the system, an apparatus, comprising:

a memory receiving update data from the processor during a first time period at a data rate corresponding to the clock and outputting the update data to the updatable table;

a control circuit coupled to the memory, wherein the control circuit determines the beginning of a second period of time during which the updatable table is not being used and updates the updatable table during the second period, asynchronously with the clock, using at least some of the update data.

20. (originally presented) Apparatus, as claimed in line 19, further comprising a plurality of shadow registers wherein data stored in the memory at a first storage time is also stored in at

least one of the plurality of shadow registers substantially simultaneously with the first storage time.

21. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table comprises an updatable transmit table and updatable receive table, and wherein the memory includes at least a transmit holding memory for holding data for updating the updatable transmit table and a receive holding memory, different from the transmit holding memory, for holding data for updating the updatable receive table.

22. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table comprises a switch table.

23. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table comprises a routing table.

24. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table controls the routing of isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, on a bus.

25. (originally presented) Apparatus, as claimed in claim 24, wherein the isochronous data comprises telephony data, video data, or a combination of telephony data and video data.

26. (originally presented) Apparatus, as claimed in claim 24, wherein the non-isochronous data comprises packet data.

27. (originally presented) Apparatus, as claimed in claim 24, wherein the non-isochronous data comprises Ethernet data.

28. (originally presented) Apparatus, as claimed in claim 24, wherein the non-isochronous data comprises non-packet, non-isochronous data.

29. (originally presented) Apparatus, as claimed in claim 24, wherein the non-isochronous data comprises ATM data.

30. (originally presented) Apparatus, as claimed in claim 24, wherein the bus comprises a time division multiplexed bus.

31. (originally presented) Apparatus, as claimed in claim 24, wherein the bus comprises a time slot interchange bus.

32. (originally presented) Apparatus, as claimed in claim 24, wherein the bus comprises a bus for carrying ATM, SONET or 1394 data.

33. (originally presented) Apparatus, as claimed in claim 24, wherein the bus connects multiple hubs in the system.

34. (originally presented) Apparatus, as claimed in claim 19, wherein the memory comprises a register.

35. (previously amended) Apparatus, as claimed in claim 19, wherein the memory comprises a random access memory (RAM).

36. (originally presented) Apparatus, as claimed in claim 19, wherein the memory comprises a multi-port memory.

37. (originally presented) Apparatus, as claimed in claim 19, wherein update data is transferred to the memory in the form of a burst.

38. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table operates synchronously with a second clock.

39. (originally presented) Apparatus, as claimed in claim 38, wherein the second clock comprises a network reference clock.

40. (originally presented) Apparatus, as claimed in claim 39, wherein the network reference clock comprises a WAN reference clock.

41. (originally presented) Apparatus, as claimed in claim 39, wherein the network reference clock comprises a LAN reference clock.

42. (originally presented) Apparatus, as claimed in claim 19, wherein the updatable table controls a hub in the system.

43. (originally presented) Apparatus, as claimed in claim 42, wherein the hub comprises a PBX.

44. (originally presented) Apparatus, as claimed in claim 42, wherein the hub includes multiple LAN connections.

45. (originally presented) Apparatus, as claimed in claim 42, wherein the hub includes multiple isochronous switching devices.

46. (originally presented) Apparatus, as claimed in claim 42, wherein the hub includes multiple Ethernet connections.

47. (originally presented) Apparatus, as claimed in claim 42, wherein the hub is coupled to multiple nodes.

48. (originally presented) Apparatus, as claimed in claim 47, wherein each of the nodes transfers isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, in the system under control of the updatable table.

49. (originally presented) Apparatus, as claimed in claim 19, wherein data transfer in the system is controlled so that bandwidth for isochronous data transfers is insensitive to a level of non-isochronous data transfers in the system.

50. (originally presented) Apparatus, as claimed in claim 19, wherein data transfer in the system is controlled so that bandwidth for non-isochronous data transfers is insensitive to a level of isochronous data transfers in the system.

51. (originally presented) Apparatus, as claimed in claim 19, wherein operations that the processor handles includes call control, signaling, maintenance activities, status processing, and error bookkeeping.

52. (originally presented) Apparatus, as claimed in claim 19, wherein the update data comprises data transmitted over a D channel.

53. (currently amended) In a computer-controlled system having a processor operating according to a clock and an updatable table operating asynchronously with the clock, the updatable table outputting control data for controlling data transfers in the system, a method, comprising:

receiving update data in a memory from the processor during a first time period <u>at a data rate corresponding to the clock</u> and outputting the update data to the updatable table; and

determining the beginning of a second period of time during which the updatable table is not being used and updating the updatable table during the second period of time, asynchronously with the clock, using at least some of the update data.

54. (originally presented) A method, as claimed in claim 53, wherein the update data includes at least one control word, indicating a table update location, and at least one data word, including data to be stored at the update location.

55. (originally presented) A method, as claimed in claim 54, wherein the update data includes more data words than control words.

56. (originally presented) A method, as claimed in claim 55, further comprising the step of incrementing the control word by a first amount to provide a new table update location for a subsequent table update.

57. (previously amended) A method, as claimed in claim 56, wherein the first amount is programmable.

58. (originally presented) A method, as claimed in claim 53, wherein the update data includes a plurality of words, each of the plurality of words having at least one bit indicating whether the word is a control word or a data word.

59. (originally presented) A method, as claimed in claim 53, wherein the update data includes a plurality of words, each of the plurality of words having at least one bit indicating whether the word is the last data word of the update data.

60. (originally presented) A method, as claimed in claim 53, further comprising the step of notifying the processor when the table update is complete.

61. (originally presented) A method, as claimed in claim 60, wherein the step of notifying comprises sending an interrupt to the processor.

62. (originally presented) A method, as claimed in claim 60, wherein, after the processor has written the update data into the memory, the processor is prevented from writing further data into the memory until after the step of notifying.

63. (originally presented) A method, as claimed in claim 53, wherein the updatable table comprises a switch table.

64. (originally presented) A method, as claimed in claim 53, wherein the updatable table comprises a routing table.

65. (originally presented) A method, as claimed in claim 53, wherein the updatable table controls the routing of isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, on a bus.

66. (originally presented) A method, as claimed in claim 65, wherein the isochronous data comprises telephony data, video data, or a combination of telephony data and video data.

67. (originally presented) A method, as claimed in claim 65, wherein the non-isochronous data comprises packet data.

68. (originally presented) A method, as claimed in claim 65, wherein the non-isochronous data comprises Ethernet data.

69. (originally presented) A method, as claimed in claim 65, wherein the non-isochronous data comprises non-packet, non-isochronous data.

70. (originally presented) A method, as claimed in claim 65, wherein the non-isochronous data comprises ATM data.

71. (originally presented) A method, as claimed in claim 65, wherein the bus comprises a time division multiplexed bus.

72. (originally presented) A method, as claimed in claim 65, wherein the bus comprises a time slot interchange bus.

73. (originally presented) A method, as claimed in claim 65, wherein the bus comprises a bus for carrying ATM, SONET or 1394 data.

74. (originally presented) A method, as claimed in claim 65, wherein the bus connects multiple hubs in the system.

75. (originally presented) A method, as claimed in claim 53, wherein the memory comprises a register.

76. (previously amended) A method, as claimed in claim 53, wherein the memory comprises a random access memory (RAM).

77. (originally presented) A method, as claimed in claim 53, wherein the memory comprises a multi-port memory.

78. (originally presented) A method, as claimed in claim 53, wherein update data is transferred to the memory in the form of a burst.

79. (originally presented) A method, as claimed in claim 53, wherein the updatable table operates synchronously with a second clock.

80. (originally presented) A method, as claimed in claim 79, wherein the second clock comprises a network reference clock.

81. (originally presented) A method, as claimed in claim 80, wherein the network reference clock comprises a WAN reference clock.

82. (originally presented) A method, as claimed in claim 80, wherein the network reference clock comprises a LAN reference clock.

83. (originally presented) A method, as claimed in claim 53, wherein the updatable table controls a hub in the system.

84. (originally presented) A method, as claimed in claim 83, wherein the hub comprises a PBX.

85. (originally presented) A method, as claimed in claim 83, wherein the hub includes multiple LAN connections.

86. (originally presented) A method, as claimed in claim 83, wherein the hub includes multiple isochronous switching devices.

87. (originally presented) A method, as claimed in claim 83, wherein the hub includes multiple Ethernet connections.

88. (originally presented) A method, as claimed in claim 83, wherein the hub is coupled to multiple nodes.

89. (originally presented) A method, as claimed in claim 88, wherein each of the nodes transfers isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, in the system under control of the updatable table.

90. (originally presented) A method, as claimed in claim 53, wherein data transfer in the system is controlled so that bandwidth for isochronous data transfers is insensitive to a level of non-isochronous data transfers in the system.

91. (originally presented) A method, as claimed in claim 53, wherein data transfer in the system is controlled so that bandwidth for non-isochronous data transfers is insensitive to a level of isochronous data transfers in the system.

92. (originally presented) A method, as claimed in claim 53, wherein operations that the processor handles includes call control, signaling, maintenance activities, status processing, and error bookkeeping.

93. (originally presented) A method, as claimed in claim 53, wherein the update data comprises data transmitted over a D channel.

94. (currently amended) Apparatus for communicating between at least first and second stations in a data communication system over at least a first link, the data communication system including a plurality of data sources and sinks, at least a first of the sources and sinks configured

to receive or transmit data isochronously and a second of the sources and sinks configured to transmit data non-isochronously, the apparatus comprising:

at least a receiver and at least a first transmitter in the first station;

the first link coupling the first station with the second station;

the second station being coupled to both the first and second of the sources and sinks;

a second transmitter in the second station for transmitting data to the first receiver;

a first multiplexer in the second station for permitting the transmitting of data from both of the first and second sources and sinks over the first link as first multiplexed data, the multiplexer providing a first bandwidth for first data originating from an isochronous source, including at least the first of the sources and sinks;

at least a first updatable switch table in the first station for storing information indicating at least the destination of data;

a processor operating according to a first clock, coupled to the updatable switch table, the updatable switch table operating according to a second clock asynchronously with the first clock;

a memory coupled to the processor receiving update data from the processor during a first time period at a data rate corresponding to the clock and coupled to the first updatable switch table and outputting the update data to the first updatable switch table.

95. (originally presented) Apparatus, as claimed in claim 94, wherein data transfer in the system is controlled so that bandwidth for isochronous data transfers is insensitive to a level of non-isochronous data transfers in the system.

96. (originally presented) Apparatus, as claimed in claim 94, wherein data transfer in the system is controlled so that bandwidth for non-isochronous data transfers is insensitive to a level of isochronous data transfers in the system.

97. (currently amended) A method for communicating data over a data link in a data communication system between a first station coupled to a first endpoint of the data link and a second station coupled to a second endpoint of the data link, the second station having an isochronous data source, a non-isochronous data source or both an isochronous data source and a non-isochronous data source, the data communication system having a time-varying amount of non-isochronous demand, the method comprising;

time-division multiplexing data from the isochronous data source and/or the non-isochronous data source, wherein a first bandwidth is allocated for data from the isochronous source, wherein the data transfer rate for the isochronous data is substantially independent of the non-isochronous demand on the data system;

providing a processor in the first station operating according to a first clock and an updatable table operating according to a second clock asynchronously with the first clock;

receiving update data in a memory from the processor during a first time period at a data rate corresponding to the clock, the update data including at least destination data;

updating the updatable table asynchronously with the first clock, using at least some of the update data in the memory; and

transmitting the time-multiplexed data onto the data link in accordance with data stored in the updatable table.

98. (originally presented) A method, as claimed in claim 97, wherein the step of updating comprises:

sampling the second clock;

providing the sampled second clock to a circuit whose output has a corresponding relationship to the rising edge of the second clock.

99. (originally presented) A method, as claimed in claim 97, further comprising the step of:

waiting up to a predetermined maximum wait time before performing the step of receiving update data if fewer than a predetermined number of update words are contained in the update data.

100. (originally presented) A method, as claimed in claim 99, wherein the predetermined number of update words is equal to the number of words that can be stored in the memory.

101. (originally presented) A method, as claimed in claim 97, wherein the update data includes at least one control word, indicating a table update location, and at least one data word, including data to be stored at the update location.

102. (originally presented) A method, as claimed in claim 101, wherein the update data includes more data words than control words.

103. (originally presented) A method, as claimed in claim 102, further comprising the step of incrementing the control word by a first amount to provide a new table update location for a subsequent table update.

104. (previously amended) A method, as claimed in claim 103, wherein the first amount is programmable.

105. (originally presented) A method, as claimed in claim 97, wherein the update data includes a plurality of words, each of the plurality of words having at least one bit indicating whether the word is a control word or a data word.

106. (originally presented) A method, as claimed in claim 97, wherein the update data includes a plurality of words, each of the plurality of words having at least one bit indicating whether the word is the last data word of the update data.

107. (originally presented) A method, as claimed in claim 97, further comprising the step of notifying the processor when the table update is complete.

108. (originally presented) A method, as claimed in claim 107, wherein the step of notifying comprises sending an interrupt to the processor.

109. (originally presented) A method, as claimed in claim 107, wherein, after the processor has written the update data into the memory, the processor is prevented from writing further data into the memory until after the step of notifying.

110. (originally presented) A method, as claimed in claim 97, wherein the updatable table comprises a switch table.

111. (originally presented) A method, as claimed in claim 97, wherein the updatable table comprises a routing table.

112. (originally presented) A method, as claimed in claim 97, wherein the updatable table controls the routing of isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, on a bus.

113. (originally presented) A method, as claimed in claim 112, wherein the isochronous data comprises telephony data, video data, or a combination of telephony data and video data.

114. (originally presented) A method, as claimed in claim 112, wherein the non-isochronous data comprises packet data.

115. (originally presented) A method, as claimed in claim 112, wherein the non-isochronous data comprises Ethernet data.

116. (originally presented) A method, as claimed in claim 112, wherein the non-isochronous data comprises non-packet, non-isochronous data.

117. (originally presented) A method, as claimed in claim 112, wherein the non-isochronous data comprises ATM data.

118. (originally presented) A method, as claimed in claim 112, wherein the bus comprises a time division multiplexed bus.

119. (originally presented) A method, as claimed in claim 112, wherein the bus comprises a time slot interchange bus.

120. (originally presented) A method, as claimed in claim 112, wherein the bus comprises a bus for carrying ATM, SONET or 1394 data.

121. (originally presented) A method, as claimed in claim 112, wherein the bus connects multiple hubs in the system.

122. (originally presented) A method, as claimed in claim 97, wherein the memory comprises a register.

123. (previously amended) A method, as claimed in claim 97, wherein the memory comprises a random access memory (RAM).

124. (originally presented) A method, as claimed in claim 97, wherein the memory comprises a multi-port memory.

125. (originally presented) A method, as claimed in claim 97, wherein update data is transferred to the memory in the form of a burst.

126. (originally presented) A method, as claimed in claim 97, wherein the updatable table operates synchronously with the second clock, the second clock having a different frequency than the first clock.

127. (originally presented) A method, as claimed in claim 97, wherein the second clock comprises a network reference clock.

128. (originally presented) A method, as claimed in claim 127, wherein the network reference clock comprises a WAN reference clock.

129. (originally presented) A method, as claimed in claim 127, wherein the network reference clock comprises a LAN reference clock.

130. (originally presented) A method, as claimed in claim 97, wherein the updatable table controls a hub in the system.

131. (originally presented) A method, as claimed in claim 130, wherein the hub comprises a PBX.

132. (originally presented) A method, as claimed in claim 130, wherein the hub includes multiple LAN connections.

133. (originally presented) A method, as claimed in claim 130, wherein the hub includes multiple isochronous switching devices.

134. (originally presented) A method, as claimed in claim 130, wherein the hub includes multiple Ethernet connections.

135. (originally presented) A method, as claimed in claim 130, wherein the hub is coupled to multiple nodes.

136. (originally presented) A method, as claimed in claim 135, wherein each of the nodes transfers isochronous data, non-isochronous data, or a combination of isochronous data and non-isochronous data, in the system under control of the updatable table.

137. (originally presented) A method, as claimed in claim 97, wherein data transfer in the system is controlled so that bandwidth for isochronous data transfers is insensitive to a level of non-isochronous data transfers in the system.

138. (originally presented) A method, as claimed in claim 97, wherein data transfer in the system is controlled so that bandwidth for non-isochronous data transfers is insensitive to a level of isochronous data transfers in the system.

139. (originally presented) A method, as claimed in claim 97, wherein operations that the processor handles includes call control, signaling, maintenance activities, status processing, and error bookkeeping.

140. (originally presented) A method, as claimed in claim 97, wherein the update data comprises data transmitted over a D channel.